High Power Factor Single Stage Flyback Converter for Dimmable LED Driver

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Abstract –Single stage Flyback converter with active power factor correction (PFC) function built-in is very popular for low power LED driver application. However, a universal driver design (120V~277Vac wide input) for meeting PF>0.90 and THD<20% at 50% of maximum output power remains very challenging using peak current transition mode (PCTM) PFC control. Therefore, in this paper, a novel and practical scheme is presented for a single stage Flyback LED driver to achieve high power factor for universal input. Based on LED output feedback, the off-time is controlled to operate the Flyback converter in discontinuous conduction mode (DCM) to realize high PF. The control implementation can be adapted to existing popular PCTM PFC controller and due to the secondary side current regulation, it is suitable for dimmable LED driver application. A 22W dimmable LED driver is prototyped to verify this scheme and at 10W output power, PF>0.90 and THD<20% are achieved for the universal input voltage range.

***Index Terms*—Power Factor Correction, Universal AC Input, Dimmable LED Drivers, Small Signal Model, Flyback Converter Modeling, Off-time control.**

I. INTRODUCTION

The penetration of LED-based solid state lighting is deeper and deeper to both residential and commercial applications. Regulators have been working with utilities companies to set stricter standards to regulate the impacts of solid state lighting (SSL) technology on the power grid. Although the adoption to LED-based SSL offers significantly reduced active power consumption, if power factor is not well managed, the grid will still need to provide a higher apparent power due to the circulating reactive power. This fact eliminates a significant portion of the benefits of LED lighting.

Table 1 shows the recent requirements for system efficiency, *PF* and total harmonic distortion (*THD*) in different regions of the world. It is believed that the requirement for residential applications is coming, due to the increasing total power level of LED lighting installed in such applications.

There are many different methods of controlling the power converter to achieve *PFC* [3]. For low power Boost *PFC*, constant t_{ON} and peak current control are the most commonly used methods and the Boost *PFC* often operates in transition mode (TM) or boundary conduction mode (BCM). For high power application, CCM (continuous conduction mode) operation is often used to reduce the inductor peak current and average current mode control can be used to achieve high *PF*. Furthermore, fixed off time (FOT) control was reported in [4][5] for Boost *PFC*. In [4], the Boost converter is operated in different modes, i. e., TM, BCM and CCM within the half line cycle. In order to make the off-time a function of input rms voltage, the input sense circuitry will modulate the off-time. This technique is suitable for a Boost *PFC* in hundred-watt level and the implementation is based on a peak current mode controller, which fills the application gap between CCM and TM *PFC*. The CCM FOT method discussed in [5] provides the off-time modulated with the instantaneous line voltage and the resulting switching frequency is constant and not dependent on the rms input voltage or on the output load. However, these two FOT methods are not suitable for low power, say, 20W *PFC* application and cannot be directly applied to single stage Flyback *PFC* for LED driver.

Table 1 Requirements for system efficiency, *PF* and total harmonic distortion (*THD*) in different regions of the world [1][2]

		US			Europe	China	Korea	Japan
		DOE	Energy Star	California				
Residential	Efficiency	50lm/W	50lm/W	N/A	N/A	N/A	N/A	N/A
	PF	>0.70	>0.70	N/A	>0.70	N/A	>0.85	N/A
	THD	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Commercial	Efficiency	55lm/W	55lm/W	55lm/W	N/A	N/A	N/A	N/A
	PF	>0.90	>0.90	>0.90	>0.90	>0.90	>0.90	>0.90
	THD	<20%	<20%	<20%	<20%	<30%	<30%	<30%

For Flyback *PFC* on the other hand, using peak current control or constant t_{ON} control in TM/BCM, the performance is usually worse than that of the Boost *PFC* especially for universal line input at 277V for low power application. Analysis is conducted in this paper to theoretically explain the reason of worse *PF* performance in TM/BCM Flyback *PFC* using peak current control or constant t_{ON} control. So constant t_{ON} +constant frequency control was introduced to maximize the *PF* to close to 1 for Flyback *PFC*. In the control scheme, a certain type of voltage controlled oscillator (VCO) is required and a practical discrete implementation will add complexity and limitation to the control scheme. Therefore, most of such solutions are built into a primary side regulation (PSR) controller, which usually requires mixed signal processing capability inside the IC and results in higher cost. Also for dimmable LED driver application, PSR is not possible to achieve very tight output current regulation (<2%) in the whole operation window of the driver. Therefore, in this paper, a novel and practical adjustable off-time control is proposed and designed for the most popular and cost efficient peak current mode control *PFC* IC to achieve high *PF* and tight current regulation for a secondary current regulation controlled single stage Flyback LED driver.

II. BASIC IDEA OF THE PROPOSED CONTROL METHOD

In Figure 1, a typical Boost *PFC* and the control scheme elements are shown [3]. The output voltage of the *PFC* will be sensed and fed into the error amplifier (EA) for compensation. The sinusoidal reference comes from the rectified line voltage and it is multiplied with the EA output in the multiplier. The output from the multiplier will be the peak current reference to control the switching of the *PFC* MOSFET and the reference can be calculated in equation **(1)**. When the sensed peak current signal (CS) of the MOSFET reaches the reference from the multiplier, the MOSFET will be turned off. The zero current detection (*ZCD*) circuit receives the demagnetizing signal from the auxiliary winding, and determines the moment when the *PFC* inductor current goes to zero. And the negative-going V_{zcd} signal will turn on the MOSFET for the next switching cycle. The inductor current i_L, peak current i_{L_peak} and average current i_{L_avg} are shown in Figure 1. The average i_{L_avg} can be calculated in equation **(2)**, where $v_{in}(t)$ is the instant rectified input voltage. V_{EA} is the error amplifier output. R_{sense} is the sensing resistance and $\frac{1}{k}$ is the gain of the sinusoidal reference. Because of the low bandwidth of the compensation network (typically ~10Hz), V_{EA} can be considered as a constant *DC* signal. The average current can be finally simplified as a product of a constant K_{PFC} and the input voltage, which explains the good *PF* performance of the peak current control in Boost converter.

$$I_{ref\_peak}(t) = \frac{1}{k} v_{in}(t) \cdot V_{EA} \tag{1}$$

$$I_{L\_avg}(t) = \frac{I_{ref\_peak}}{2} = \frac{1}{k} \frac{v_{in}(t) \cdot V_{EA}}{2R_{sense}} = K_{PFC} v_{in}(t) \tag{2}$$

$$t_{OFF}(t) = \frac{t_{ON} \cdot v_{in}(t)}{N_{ps}(V_{out} + V_F)} \tag{3}$$

Peak current control and constant t_{ON} control are widely used in Boost *PFC* due to the aforementioned good *PF* performance and relatively mature IC solutions [13]. However, the direct adaptation to Flyback *PFC* operated in TM/BCM will not achieve good *PF* performance. Use constant t_{ON} control on Flyback as an example, the off-time t_{OFF} can be estimated using equation **(3)**, where N_{ps} is the turns ratio between primary and secondary side windings and V_F is the forward voltage drop of the output rectifier diode. The average input current of the constant t_{ON} controlled Flyback can be calculated as equation **(4)**. It can be observed that the average current cannot be written as a product of a constant and $v_{in}(t)$, which explains poor *PF*. Peak current controlled Flyback *PFC* will have the same issue [14].

Even though in the design we can make the Flyback reflected voltage $N_{ps}(V_{out} + V_F) \gg v_{in}(t)$ to improve the *PF* as shown in equation **(5)**, it is not practical due to the higher voltage stress on the Flyback MOSFET and/or higher current stress on the output diode.

Inspired from equation **(4)**, if both on-time (t_{ON}) and switching period (t_{ON}+t_{OFF}) are made constant at the same time, good *PF* can be achieved. With this approach, the internal current loop can be completely eliminated, so that the converter will be operated at constant on-time and constant switching frequency for a concern operating condition of I_{out} and V_{out}. With the converter working in DCM, this control technique allows unity power factor when used with converter topologies like Flyback, Cuk and SEPIC [4]-[10]. Instead, with the Boost *PFC,* this technique causes some harmonic distortion in the line current [3][11].

One existing solution to implement equation **(5)** for a DCM Flyback *PFC* is to control t_{ON} using PSR and control switching frequency according to V_{out} at the same time [12]. Besides the PSR tolerance issue mentioned before, in a practical IC implementation, the LED output voltage range is always limited by the internal voltage controlled oscillator (VCO) frequency range (V_{out_max}:V_{out_min}<2:1) [12]. On the other hand, in the proposed method, t_{OFF} is regulated as a constant for a certain operating condition to implement equation **(4)** for a wider V_{out} range (V_{out_max}:V_{out_min}>2:1). The proposed method can be adapted to secondary side regulated (SSR) single stage Flyback LED driver to achieve tighter regulation requirement for dimming application. Also cost wise, due to the mixed signal core of primary side controller, it is cheaper to have an improved method for peak current controlled Flyback *PFC* using more popular *PFC* ICs, such as [13].

$$i_{L\_avg}(t) = \frac{1}{2} \frac{t_{ON} \cdot i_{L\_peak}}{t_{ON} + t_{OFF}(t)} = \frac{1}{2L} \frac{t_{ON} \cdot v_{in}(t) \cdot N_{ps}(V_{out} + V_F)}{v_{in}(t) + N_{ps}(V_{out} + V_F)} \tag{4}$$

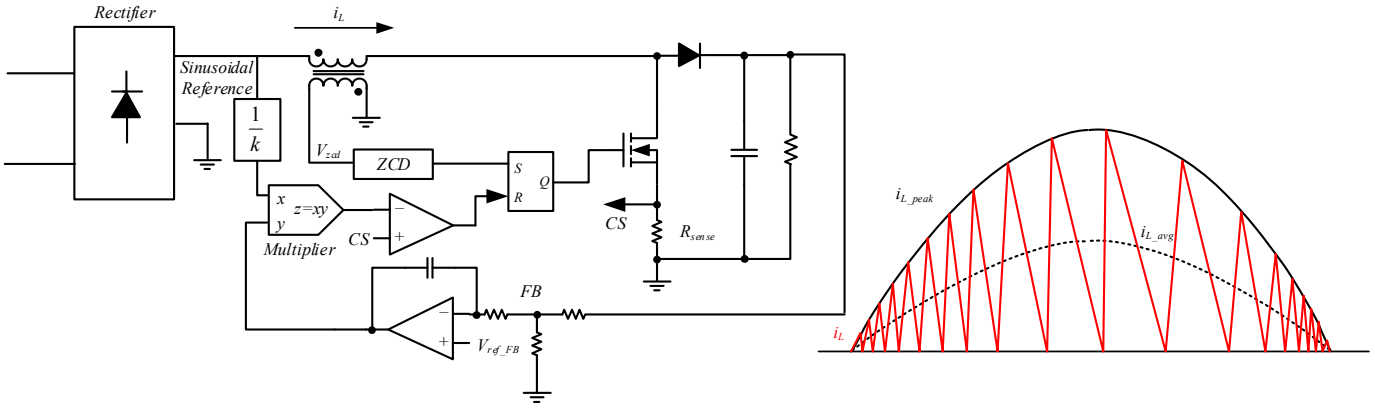

Figure 1 Proposed system and functional Blocks

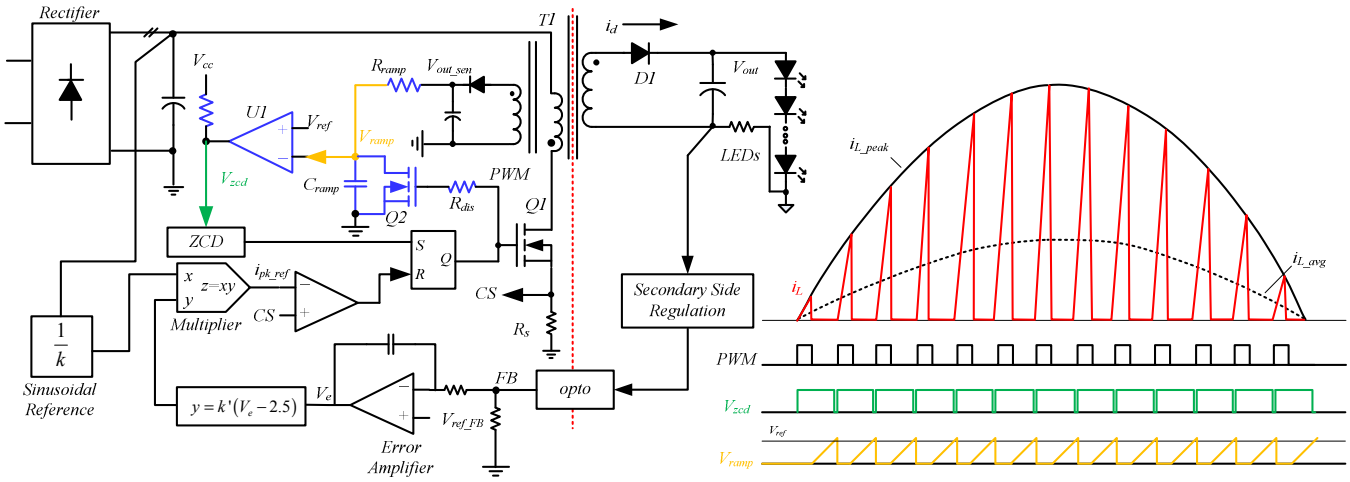

Figure 2 Proposed adjustable T_{off} control diagram for Flyback PFC

$$\lim_{N_{ps}(V_{out}+V_F)\to\infty}\left[i_{L\_avg}(t)\right] = \lim_{N_{ps}(V_{out}+V_F)\to\infty}\left[\frac{1}{2}\frac{t_{ON}\cdot i_{L\_peak}}{t_{ON}+t_{OFF}(t)}\right] = \frac{t_{ON}\cdot v_{in}(t)}{2L} \quad (5)$$

III. DESIGN ANALYSIS AND GUIDELINES

Even though the proposed method can be implemented in PSR as well, due to tighter output regulation requirement in dimming application (<2%), in Figure 2, the current regulation is implemented on the secondary side to achieve the goal. The FB signal from the opto-coupler will be regulated according to the reference V_{ref_FB} of the error amplifier (EA). Similar to peak current control, the sinusoidal reference will be sensed and multiplied with the EA output to create the peak current reference (called i_{pk_ref}) and i_{pk_ref} can be calculated in **(6)**. In this implementation, the IC used [13] will condition the V_e signal using the equation $y = k' \cdot (V_e - 2.5)$ internally shown in Figure 2, where k'=0.38 (typical value) in the specification. When the current sensing signal CS is higher than i_{pk_ref}, the PWM signal will be low to turn off the MOSFET Q1.

$$i_{pk\_ref}(t) = \frac{\sqrt{2}V_{in}\sin t}{k}\cdot k'\cdot(V_e - 2.5) \quad (6)$$

The adjustable T_{off} control element is highlighted in blue and consists of U1, Q2, R_{ramp}, C_{ramp}, R_{dis}, etc. When the MOSFET Q1 is turned off, the capacitor C_{ramp} is charged up from V_{out_sen} via R_{ramp}, where V_{out_sen} is proportional to output voltage V_{out}. When the voltage V_{ramp} is higher than V_{ref}, the V_{zcd} will be pulled low. After a delay from *ZCD* block, the MOSFET Q1 will be turned on again for the next switching cycle. And at the same time, the signal FET Q2 will be turned on as well to discharge C_{ramp} and reset the V_{zcd} to high. When the V_{out} is higher (and I_{out} remains the same), the charging process of the C_{ramp} is faster to create shorter T_{off} and vice versa. If the I_{out} is increased (and V_{out} remains the same), T_{off} will be the same but T_{on} will be longer and vice versa. The on-time T_{on} can be solved from equation **(7)**, where L_m is the magnetizing inductance of T1. The Flyback converter will be

always operated in DCM by designing of a proper T1 and the T_{off} timing control circuit.

$$T_{on} = \frac{L_m (V_e - 2.5) k'}{k \cdot R_s} \quad (7)$$

$$T_{off} = R_{ramp} C_{ramp} \ln\left(1 - \frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay} \quad (8)$$

To design the Flyback transformer for DCM operation, the transformer demagnetizing time T_{dis} (T_{dis} is defined as the interval from the moment when D1 conducts to the moment when i_d=0, so T_{dis} is different from T_{off}.) has to be smaller than the controlled off-time in the timing circuit. In this proposed scheme, the T_{off} is mainly controlled by V_{out_sen}, R_{ramp} and C_{ramp}. And T_{off} can be estimated as in **(8)**, where t_{delay} is the delay between the moment when V_{ramp}>V_{ref} and Q1 is turned on. In this prototype, the targeted minimum voltage V_{out_min} is 15V and maximum voltage V_{out_max} is 30V, while output current is 70mA (I_{out_min}) to 700mA (I_{out_max}). The minimum switching frequency is set as 25kHz to avoid audible noise. The maximum inductance can be calculated in **(9)** at V_{out_min} and I_{out_max}, where f_{sw} is the switching frequency and η is the efficiency.

$$L_{\max} = \frac{V_{inrms\_\min}^{\ 2} \cdot T_{on}^{\ 2} \cdot f_{sw} \cdot \eta \cdot PF}{V_{out\_\min} \cdot I_{out\_\max}} \quad (9)$$

In Figure 3, the off-times are plotted for 15V (5 LEDs, assuming 3V per LED) and 27V (9 LEDs) with R_{ramp}=10kΩ, C_{ramp}=11nF, and t_{delay} of *ZCD* block is about 1.4us. And the T_{dis} is calculated for different output LED voltages and currents in each of the cases, the curve of T_{dis} has to be lower than off-time (dashed) for the same input rms and output LED voltages to achieve DCM. Switching frequency curves are also calculated to show that the lowest output voltage can be reached for this R_{ramp} and C_{ramp} combination is <10V and the switching frequency is still higher than 25kHz to avoid audible noise.

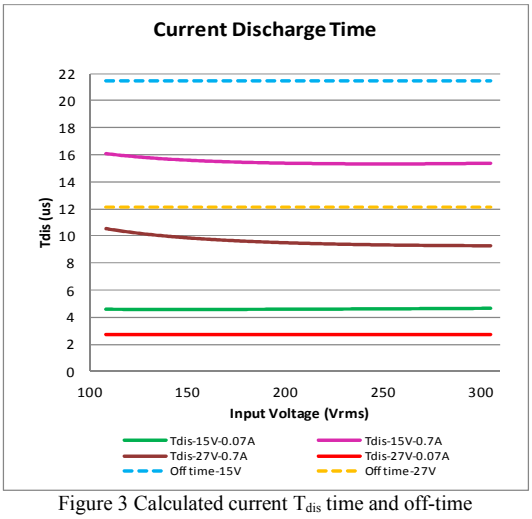

Figure 3 Calculated current T_{dis} time and off-time

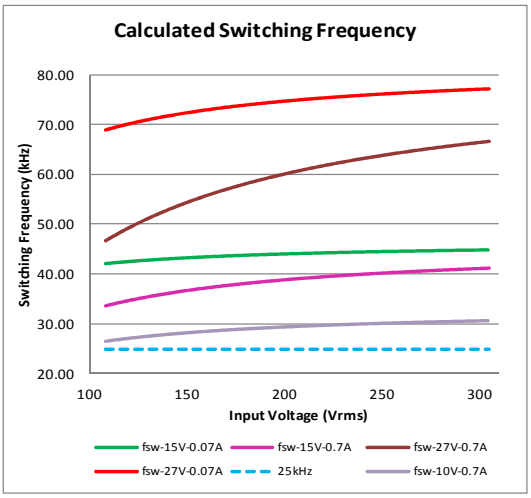

Figure 4 Calculated Switching Frequency of the proposed scheme

IV. Small Signal Modeling

The average large-signal model of a peak current controlled Flyback converter can be obtained by replacing the semiconductors Q1 and D1 in Figure 2 with dependent current sources [14]-[19]. I_p is the average peak current of the MOSFET Q1. The average output diode current I_d can be calculated in equation **(10)**, where V_F is the forward voltage of D1, V_o is the output voltage, and V_{in} is the AC input rms voltage.

$$I_d(V_{in}, V_o, V_e) = \frac{1}{2} \frac{\left(\frac{k'}{k}\right)^2 (V_e - 2.5)^2 L_m V_{in}^{\ 2}}{R_s^{\ 2} (V_o + V_F)\left[\frac{k'(V_e - 2.5) L_m}{k R_s} - R_{ramp} C_{ramp} \ln\left(1 - \frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right]} \quad (10)$$

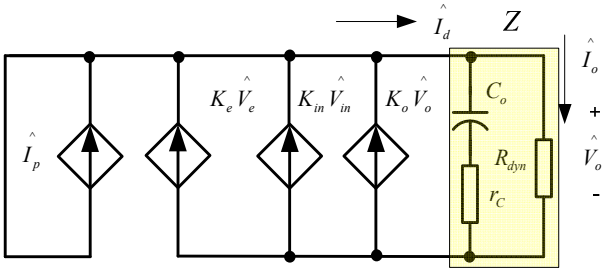

Figure 5 Small Signal Model

The small signal model can be obtained by setting all *DC* source values to zero (in Figure 5). Then I_d is linearized around its steady state operating point in **(11)**, where $K_e = \frac{\partial I_d}{\partial V_e}$, $K_{in} = \frac{\partial I_d}{\partial V_{in}}$, and $K_o = \frac{\partial I_d}{\partial V_o}$. The equations of K_e, K_{in}, and K_o for a Flyback converter are presented in (**13**)-(**15**).

$$\hat{I}_d = K_e \hat{V}_e + K_{in} \hat{V}_{in} + K_o \hat{V}_o \quad (11)$$

The DC operating point of V_e can be solved from **(12)**, where P_{out} is the output power. For example, for 120V input at full power, V_e=3.441V and for 277V input at full power V_e=2.81V. By using the DC operating point of V_e, we can calculate the gains of K_e, K_{in} and K_o for different input and output conditions.

$$\frac{P_{out}}{\eta \cdot PF \cdot V_{in}} = \frac{\left(\frac{k'}{k}\right)^2 (V_e - 2.5)^2 L_m V_{in}}{2R_s^2} \Bigg/ \left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right] \tag{12}$$

$$K_e = \frac{V_{in}^2\left(\frac{k'}{k}\right)^2 L_m (2V_e - 5)}{2R_s^2 (V_o + V_F)^2} \Bigg/ \left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right] \tag{13}$$

$$- \frac{V_{in}^2\left(\frac{k'}{k}\right)^3 L_m^2 (V_e-2.5)^2}{2R_s^3 (V_o + V_F)} \Bigg/ \left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right]^2$$

$$K_{in} = \frac{V_{in}\left(\frac{k'}{k}\right)^2 L_m (V_e-2.5)^2}{R_s^2 (V_o + V_F)} \Bigg/ \left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right] \tag{14}$$

$$K_o = \frac{V_{in}^2\left(\frac{k'}{k}\right)^2 L_m (V_e-2.5)^2}{2R_s^2 (V_o + V_F)^2} \Bigg/ \left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right] \tag{15}$$

$$- \frac{V_{in}^2\left(\frac{k'}{k}\right)^2 L_m^2 (V_e-2.5)^2 R_{ramp}C_{ramp}V_{ref}}{2R_s^2 V_o^2 (V_o + V_F)} \Bigg/ \left(\frac{V_{ref}}{V_{out\_sen}} - 1\right)\left[\frac{k'}{k}\frac{(V_e-2.5)L_m}{R_s} - R_{ramp}C_{ramp}\ln\left(1-\frac{V_{ref}}{V_{out\_sen}}\right) + t_{delay}\right]^2$$

The transfer function from error voltage $\hat{V}_e$ to output current $\hat{I}_o$ is obtained in equation (**16**), where Z is the output impedance in equation (**17**) and R_{dyn} is the LED dynamic resistance [20].

$$G_{ie} = \left.\frac{\hat{I}_o}{\hat{V}_e}\right|_{\hat{V}_{in}=0} = \frac{Z \cdot K_e}{R_{dyn} \cdot (1 - Z \cdot K_o)} \tag{16}$$

$$Z = \frac{R_{dyn}\left(1 + s \cdot C_o \cdot r_C\right)}{1 + s \cdot C_o \cdot \left(r_C + R_{dyn}\right)} \tag{17}$$

Bode plot of G_{ie} for the proposed adjustable T_{off} control is shown in Figure 6 and Figure 7 at different input voltages, output voltages and currents. When the Flyback stage is operating at $V_{LED\min}$ (5 LEDs), the *DC* gain is higher, compared with $V_{LED\max}$ (9 LEDs). This explains that using the same compensator, Flyback LED driver stage is less stable when powering less number of LEDs.

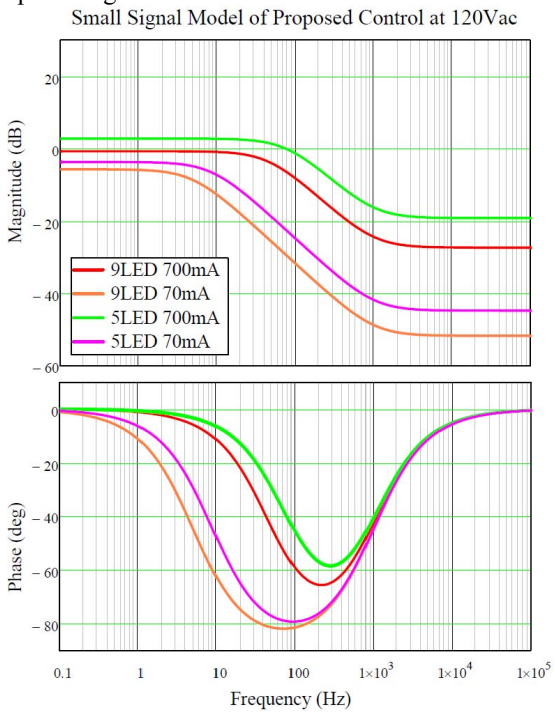

Figure 6 Bode plot of G_{ie} for proposed control scheme

At 277V AC input, the system DC gain is higher than that of the 120V AC input.

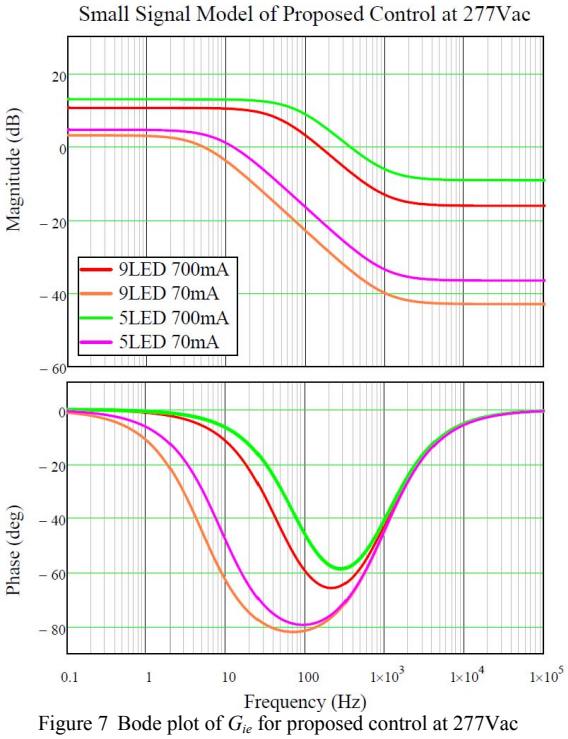

Figure 7 Bode plot of G_{ie} for proposed control at 277Vac

V. Experimental Results and Verifications

Key switching waveforms and control signals are shown in Figure 8 and Figure 9 at 277V AC input with minimum and maximum number of LED load at full load current (700mA). Ch1 is the V_{zcd} signal to the TM control IC (10V/div). Ch2 is the current of main FET Q1 (500mA/div). Ch3 is the drain-source voltage of Q1 (200V/div). Ch4 is the ramp signal of V_{ramp} (1V/div). Once the V_{ramp} reaches 2.5V, the circuit will create V_{zcd} failing edge to turn on the next switching cycle. After about 1.4us delay from *ZCD* block, the main FET turns on and V_{zcd} is pulled to high and V_{ramp} is reset to zero.

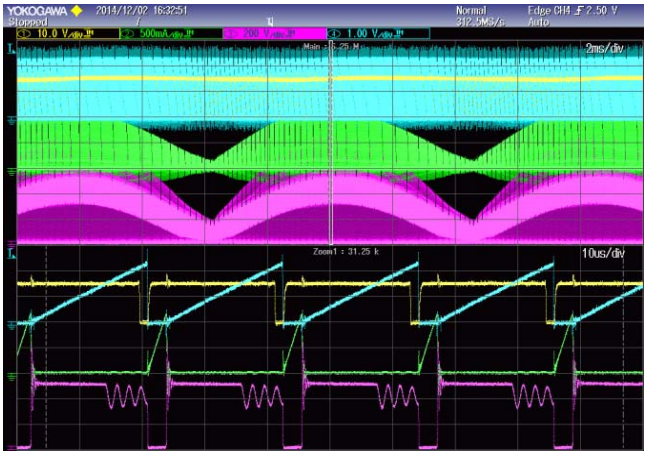

Figure 8 Experimental result of the prototype at 277V, 5 LEDs, 700mA output

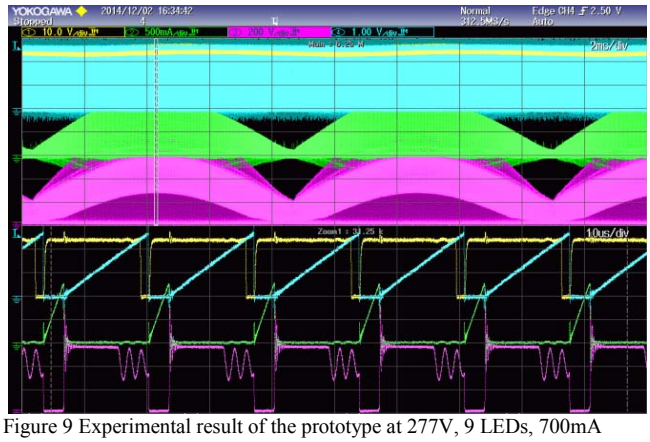

Figure 9 Experimental result of the prototype at 277V, 9 LEDs, 700mA output

It is noted that due to the higher V_{out_sen}, the T_{off} at 9 LEDs is shorter than the T_{off} at 5 LEDs. So the switching frequency at 9 LEDs output condition is about 60kHz, while the switching frequency is about 42kHz with 5 LEDs. This result is very close to the calculated result in Figure 4.

Key switching waveforms and control signals are shown in Figure 10 and Figure 11 at 277V input with minimum and maximum number of LED load at dimming current (70mA). Ch1 is the V_{zcd} signal to the TM control IC (10V/div). Ch2 is the current of main FET Q1 (500mA/div). Ch3 is the drain-source voltage of Q1 (200V/div). Ch4 is the ramp signal of V_{ramp} (1V/div). Once the V_{ramp} reaches 2.5V, the circuit will create V_{zcd} failing edge to turn on the next switching cycle. After about 1.4us delay from *ZCD* block, the main FET turns on and V_{zcd} is pulled to high and V_{ramp} is reset to zero.

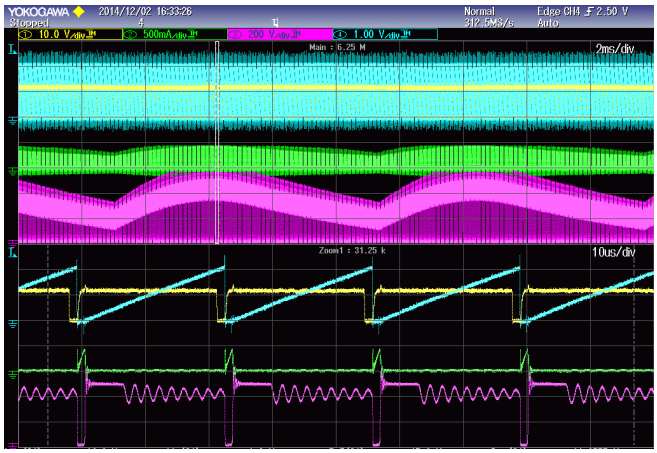

Figure 10 Experimental result of the prototype at 277V, 5 LEDs, 70mA output

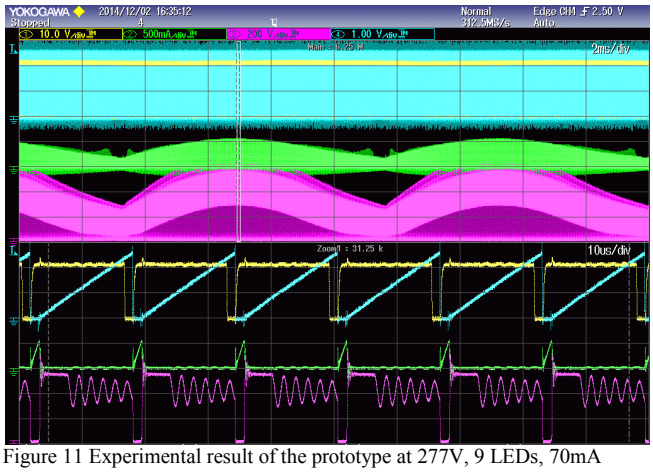

Figure 11 Experimental result of the prototype at 277V, 9 LEDs, 70mA output

It is noted that due to the higher V_{out_sen}, the T_{off} at 9 LEDs is shorter than the T_{off} at 5 LEDs. So the switching frequency at 9 LEDs output condition is about 62kHz, while the switching frequency is about 43kHz with 5 LEDs. For the same number of LEDs, switching frequency is higher in dimming condition, due to smaller T_{on}. In dimming condition, the output LED voltage and V_{out_sen} are lower compared with full current conditions, so the switching frequency is slightly lower than the calculation in Figure 4.

Key switching waveforms and control signals are shown in Figure 12-Figure 15 at 120V input with minimum and maximum number of LED load at full current (700mA) and dimming condition (70mA). Ch1 is the V_{zcd} signal to the TM control IC (10V/div). Ch2 is the current of main FET Q1 (500mA/div). Ch3 is the drain-source voltage of Q1

(100V/div). Ch4 is the ramp signal of V_{ramp} (1V/div). Once the V_{ramp} reaches 2.5V, the circuit will create V_{zcd} failing edge to turn on the next switching cycle. After about 1.4us delay from *ZCD* block, the main FET turns on and V_{zcd} is pulled to high and V_{ramp} is reset to zero.

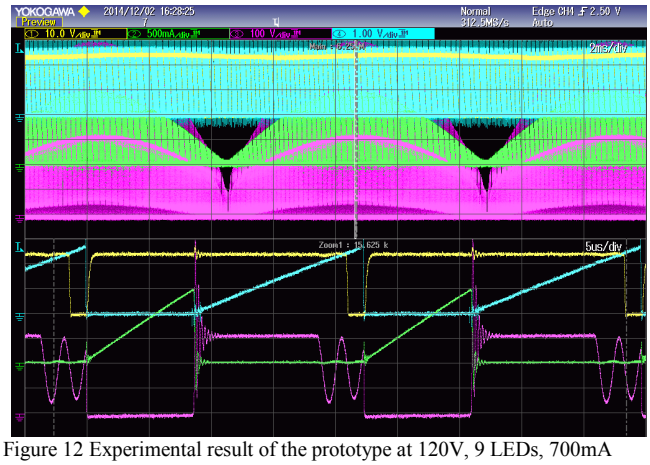

Figure 12 Experimental result of the prototype at 120V, 9 LEDs, 700mA output

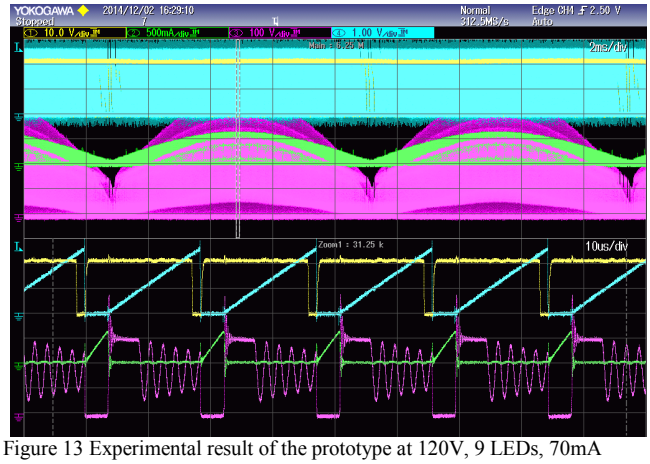

Figure 13 Experimental result of the prototype at 120V, 9 LEDs, 70mA output

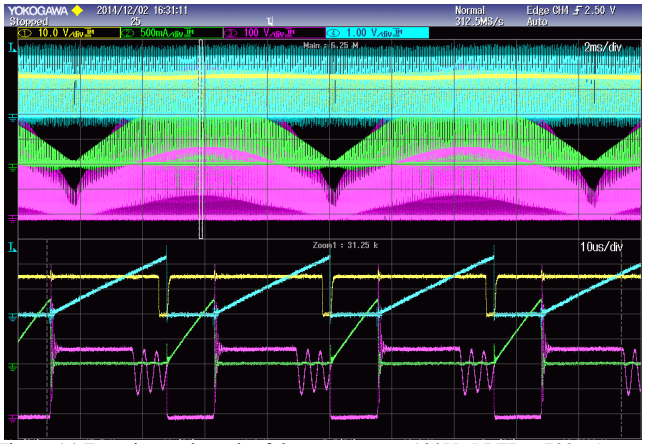

Figure 14 Experimental result of the prototype at 120V, 5 LEDs, 700mA output

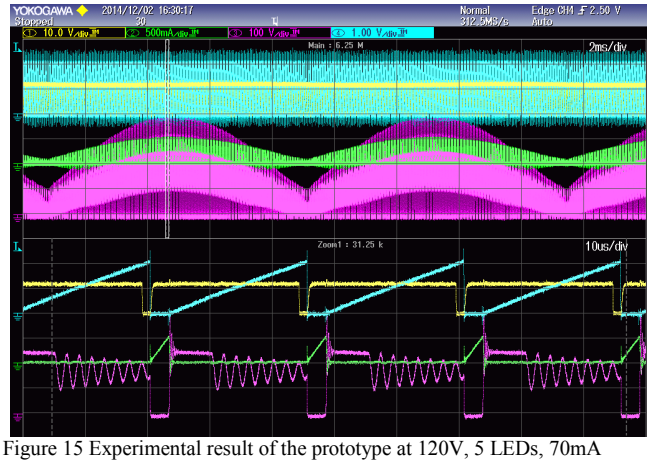

Figure 15 Experimental result of the prototype at 120V, 5 LEDs, 70mA output

In Figure 16 and Figure 17, the *PF* and *THD* plots are shown for both 120V and 277V inputs. It demonstrated that by using the proposed method, the prototype can operate from 2W to 22W by dimming control.

At 120V, within the operating range, *PF* and *THD* always meet requirements. At 277V and 10W, the *PF* is still higher than 0.90 and *THD* is lower than 20%.

PF and *THD* results using conventional PCTM controller are presented in dashed lines for comparison. At 120V input, using PCTM, the prototype will still be able to meet the *PF* and *THD* requirements, although the proposed method shows better results. However, at 277V input, the PCTM does not meet the requirement and at 15W or lower, *PF* will be lower than 0.90.

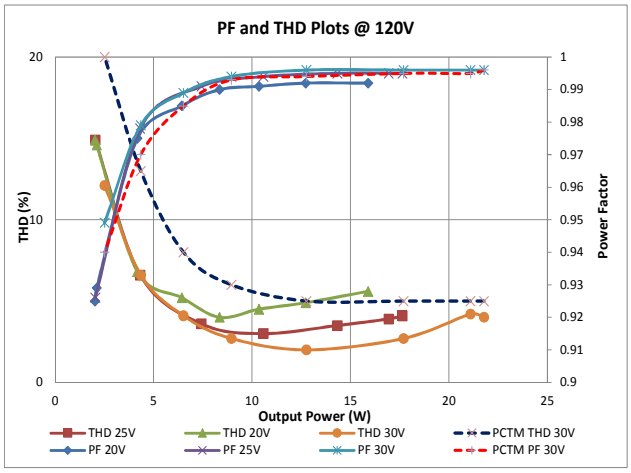

Figure 16 *PF* and *THD* plots of the prototype at 120V

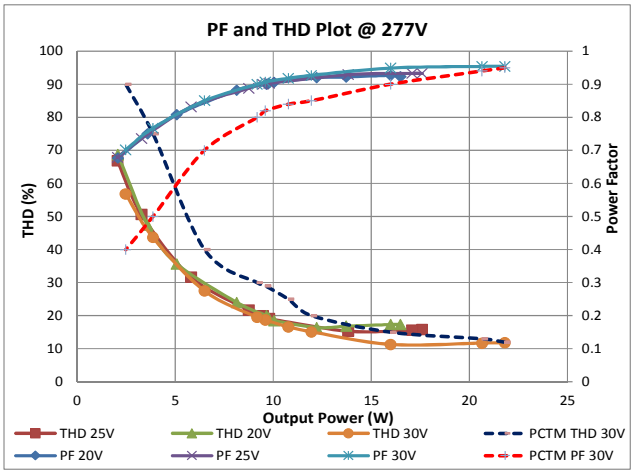

Figure 17 *PF* and *THD* plots of the prototype at 277V

VI. CONCLUSIONS

In this paper, a novel control scheme is presented for low power dimmable LED driver using single stage Flyback topology with PFC. The basic idea of the proposed scheme is outlined and compared with existing PCTM control, which is commonly used in Boost *PFC*. Implementation of the proposed method is shown in section II. , and the scheme regulates the LED current based on secondary side sensing. The off-time T_{off} is adjusted based on the V_{out} information to guarantee DCM operation for high *PF*. Detailed design guideline is provided to design the Flyback transformer and the T_{off} timing control circuit. Small signal model of the Flyback converter controlled by the proposed scheme is built and analyzed. Finally, experimental results are shown to verify the advantages of the proposed scheme in a 22W LED driver prototype. By using the proposed method, at 10W (<50% of 22W), both *PF* and *THD* meet the requirement for universal input.

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